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# Introduction

The project outlined in this report involves the construction of a Successive Approximation Analogue to Digital Converter. The circuit will take in an analogue voltage value from an on-board accelerometer and will output a digital PWM signal, via an embedded Arduino board. The report will describe the functions of the different sections of the converter, the process of building each section and its implementation, and details of how the circuit how tested. Finally, there will be a discussion of the project and what was learned.

# Acknowledgements

With thanks to Fergal Brennan and Martin Fogarty

# Project planning

A screenshot of a cell phone

Description automatically generated

# Overview of the Circuits

## Voltage Regulator

The first section of the ADC consists of a voltage regulator circuit. A voltage regulator is necessary as it important to have a steady, regular power supply to power the rest of the board. This may not be possible from a bench PSU as they are prone to excessive AC ripple. AC Ripple is the slight variation in a DC signal caused by inadequate conversion of the AC source voltage to DC [1]

The primary component in this section is an **LM7805CT**, a linear voltage regulator with fixed voltage output of 5V [2]. The **LM7805CT** is particularly efficient for this purpose as it can dissipate a lot of heat [3]. The regulator functions by essentially comparing the output voltage to a reference voltage and adjusting based on error until the required output voltage is met [4].

Decoupling capacitors are used to filter the input signal from the PSU to the regulator, and are also used on the IC’s output to filter and smooth the output signal. In the context of the full circuit, AC Ripple may potentially become a problem, as it may interfere with the very small reference voltage values output by the ramp generator and the values output by the accelerometer. Therefore it is important to filter the signals in order to reduce AC Ripple as much as possible.

A load resistor is connected to the output of the **LM7805CT** as is an LED, for testing purposes. A rectifier diode is placed on the IC input, to further reduce AC Ripple.

## Relaxation Oscillator

The next section of the ADC consists of a relaxation oscillator. The function of this relaxation oscillator is to act as a clock. The frequency of the output of this clock will determine the eventual Pulse Width Modulation frequency of the output of the comparator, which will be sent to the embedded processor.

The primary component at this stage is an **LM74AC**, a Hex Inverter with Schmitt Trigger Input. The **LM74AC** chip contains six inverter gates with Schmitt Trigger inputs [5], two of which are used in this circuit.

The first gate functions essentially as a comparator, comparing the input to the gate with negative and positive threshold voltages. According to the datasheet, the negative threshold for a 5V input is 1V, and the positive 3.55V. A capacitor is placed on the inverting input of the gate, and it is the rate of discharge/discharge of this oscillator that determines the frequency of the output of the oscillator. When the gate is powered, there will be 5V on its output which will then be fed back to the inverting input, causing the capacitor to begin charging. When the capacitor reaches 3.55V, it will then be greater than the positive threshold voltage, and so the output will switch to 0V. At that point the capacitor will begin discharging. When it discharges to the point where it is less than the negative threshold voltage, then the output will switch to 5V. In this way, a 5V square wave is generated. Schmitt Trigger inputs implement hysteresis in the form of the thresholded range of voltages described above (1V – 3.55V). This is used in order to avoid rapid fluctuations between 0V and 5V.

## Counter

In this stage of the ADC, a counter is used to create an 8-bit count from 0 to 255, which will be used to generate a ramp output from the next stage of the circuit. The main component in this section is an **SN74HC590**, an 8-bit digital counter. The clock input to this binary counter comes from the relaxation oscillator built in the previous section. The output of the oscillator was found to be [188.7kHZ](#OLE_LINK4), and so this will be twice the frequency of the Least Significant Bit (LSB) of the counter output. If we count the LSB as the “1st” bit and the MSB as the “8th”, then the nth bit will be have a frequency that is divisions of the LSB frequency, i.e:

According to the **SN74HC590** datasheet [6], the IC contains both a counter and a storage register, with a separate clock input for each of these. The counter clock is positive-edge triggered, meaning that when the oscillator transitions from low to high, the counter will increment. The clock may be reset through the !CCLR clock clear pin, or enabled through the !CCKEN clock enable pin. An RCO (Ripple Carry Output) pin may be used if multiple counters were to be chained together.

## Ramp Generator

The next section of the circuit consisted of an R2R Resistor Ladder. An R2R Ladder is essentially a series of voltage dividers that output a ramp voltage. This ramp voltage will function as a reference voltage to which the eventual output of the accelerometer will compared.

The input to the R2R ladder is the 8-bit output of the counter. This consists of 8 separate square wave signals, each half the frequency of the next. Given that these are binary signals, the R2R ladder can be thought of as functioning as a local digital-to-analogue converter [7], within the global analogue-to-digital circuit.

Each bit contributes a proportional amount of voltage to the total summed voltage at the output of the R2R ladder, resulting in a 5V sawtooth wave.

## Comparator

## Embedded Interface

## Coding

# Implementation Circuits

## Voltage Regulator

In this section of the circuit, a DC voltage is taken from a bench PSU (or battery). A ground rail is also established at this point. The input voltage is sent through first through a rectification diode, in order to alleviate AC Ripple. It is further smoothed using an input filter consisting of decoupling capacitors and finally routed through the input pin of the **LM7805CT** voltage regulator. According to the datasheet for the **LM7805CT**, the dropout voltage is 2.0V. This means that for an output of 5V, we can calculate the expected minimum required voltage from the PSU as:

According to the datasheet, the maximum input voltage should be 35V. A voltage of 12V is used, giving ample headroom on either side. The datasheet states that the output voltage tolerance is +/- 4%, and therefore we can calculate the expected output voltage range as:

The resulting 5V (+/- 4%) is routed through an output filter for smoothing and then sent through a diode and load resistor.

It is important to ensure that there are no short circuits in this section, as this may cause the **LM7805CT** to overheat due to too much current flowing through it. If the regulator overheats and enters thermal shutdown, its output voltage may drop below the required value [3].

## Relaxation Oscillator

In this second stage of the circuit, the voltage regulator output is routed to the input of a relaxation oscillator, built from an **LM74AC** IC described above. The output of this oscillator is a square wave, which has been generated via one of the inverter gates of the IC. A second inverter gate functions as a clock buffer to smooth the square wave and reduce noise.

The expected frequency output of the oscillator is a function of the time constant of the circuit and the various input and threshold voltage values [8]. Therefore, when calculating this value, the RC constant must first be determined. The resistance and capacitance of R and C were measured:

This may be compared to the labelled values of the components in order to illustrate the range of tolerance in component labelling:

The deviation between the expected and the measured may then be calculated as a percentage:

The overall output square wave frequency is determined by the following calculation:

RC was determined above to be and VCC determined to be 5.06V (see [Testing and Results – Voltage Regulator](#OLE_LINK2)). However, the VT- and VT+ values were not so easily determined as they were found to be values within a given tolerance range, according to the datasheet. Therefore, the potential output frequency had to be calculated within that range, with RC and Vcc as constants, and VT- and VT+ as variables. The calculated values are listed below (the excel table for these values may be found in the appendix):

## Counter

At this stage of the circuit, the output of the relaxation oscillator is routed to the clock input pins (CCLK/Counter and RCLK/Registry) of the **SN74HC590**. The active low CCLR/Counter Clear pin is routed to the 5V line in order to prevent the counter being cleared to 0, and the active low OE/Output Enable and CCKEN/Count Enable pins are routed to ground to ensure that the count will continue.

The **SN74HC590** will output, from 8 separate pins, parallel binary values that will constitute an 8-bit count from 0 to 255:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Decimal** | **Bit 7 (MSB)** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0 (LSB)** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| .  .  . | .  .  . | .  .  . | .  .  . | .  .  . | .  .  . | .  .  . | .  .  . | .  .  . |
| 254 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 255 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

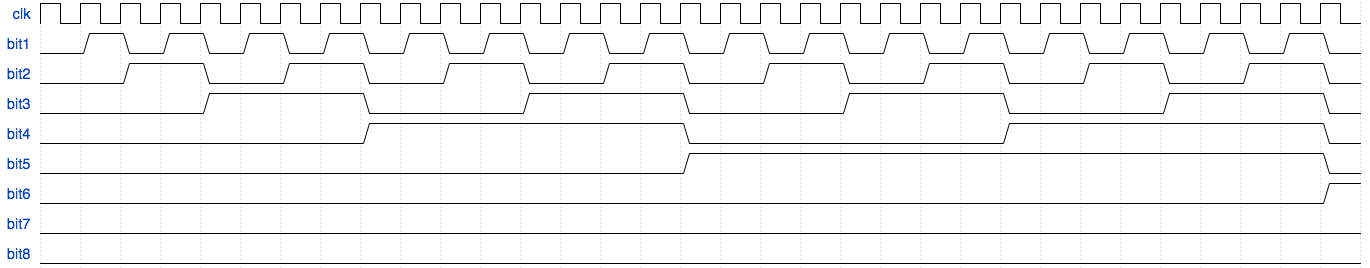
****

Figure 1: Section of 8-bit counter timing diagram

Each of these binary outputs will constitute an on/off voltage of 0V and 5V which will be fed into an R2R resistor ladder in the next stage of the circuit. The resistor ladder will take this square wave input and convert it into a ramp voltage, detailed in the next section.

## Ramp Generator

Each square wave signal from the counter, detailed in the previous section, is routed separately to the R2R ladder. The ladder is set up in such a way that each individual square wave meets a different level of impedance, which is inversely proportional to the associated bit’s significance in the overall 8-bit byte [9]. For example, the Most Significant Bit meets the minimum level of resistance and the Least Significant Bit meets the maximum level. This means that each bit allows for a voltage output proportional to its significance, i.e. MSB allows for the maximum voltage, LSB allows for the minimum.

This proportional voltage output is achieved through the ladder sequence of voltage dividers, with values of 2R for R1 and 2R (through Thevenin equivalence [10]) for R2. Each bit is connected to a voltage divider and must travel through its connected voltage divider, plus all subsequent voltage dividers. Hence, each bit voltage is successively divided, relative to its significance. For example, the LSB must travel through eight voltage dividers, which reduces its voltage by The MSB must only travel through one voltage divider, reducing its voltage by If we count the LSB as the “8th” bit and the MSB as the “1st”, then the nth bit will contribute voltage according to the following equation:

|  |  |
| --- | --- |
| **Bit number** | **Expected voltage output (when high)** |
| 1 (MSB) | = 2.53V |
| 2 | = 1.265V |
| 3 | = 0.633V |
| 4 | = 0.316V |
| 5 | = 0.158V |
| 6 | = 0.079V |
| 7 | = 0.040V |
| 8 (LSB) | = 0.020V |
| *Total (max - 255)* | 5.04V |

Table 1: Calculated voltage output values for individual bits

The resulting voltages are summed, with the maximum value of the sum being the initial square wave peak voltage of 5V. As the binary counter increments, the summing voltages increase proportionally to the bits, resulting in a ramp voltage. Given that the minimum contribution to the ramp is the input voltage having travelled through eight successive voltage dividers, the resolution of the ramp is:

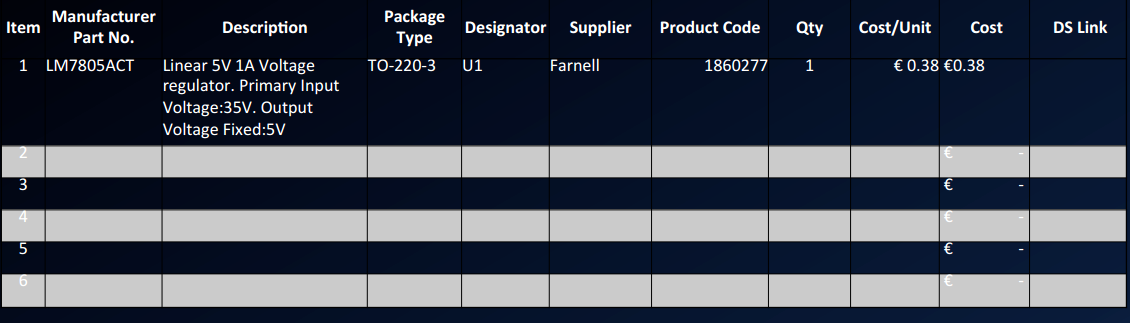
The resolution of the ramp is extremely important, as this will be the minimum voltage that can be compared with the output of the accelerometer.

The construction of the circuit involved placing the resistors according to the network structure. The R resistor value in this case was 5kΩ. Two 10kΩ resistors were used for the R value instead of a single 5kΩ resistor, as this increases tolerance from for a single resistor to .

## Comparator

## Embedded Interface

# Bill of Material



**Sellers of components Farnell, Digikey etc**

# Errors

**Only mention circuits that have or had errors. Tell the reader how you fixed the error.**

# Testing and Results

**How you tested, your results and any errors and how you fixed them.**

## Voltage Regulator

Given that the main function of the voltage regulator is to output a specified voltage, the first done was on the output voltage of this section. As calculated above (see [Implementation – Voltage Regulator),](#OLE_LINK1) the expected output was between 4.8V and 5.2V. The output voltage, when tested, was found to be 5.06V, within the expected margin of error. AC Ripple was also measured at this stage and found to be approx. 50mV. The minimum input voltage was calculated above to be approx. 7V. When measured, this value was found to be 7.23V, which was reasonably close to the expected value. The current from the bench PSU was also measured, and found to be 17.9mA

|  |  |  |
| --- | --- | --- |
| **Minimum** | **Typical** | **Maximum** |
| 7V | 12V | 35V |

Table 2: Input Voltage Values

|  |  |  |  |
| --- | --- | --- | --- |
| **Value** | **Description** | **Expected** | **Measured** |
| *Vin Min* | *Minimum input voltage* | *7V* | *7.23V* |
| *VDD* | *Output voltage* | *4.8V -> 5.2V* | *5.06V* |
| *PIN* | *Input current* | *----------* | *17.9mA* |
| *VAC RIPPLE* | *AC Ripple on input voltage* | *----------* | *50mV* |

Table 3: Test Results for Voltage Regulator

## Relaxation Oscillator

Values related to the input and output of the oscillator were tested at this stage, in order to ensure that this section of the circuit was functioning correctly. The estimated value for the output frequency was (see [Implementation – Relaxation Oscillator](#OLE_LINK3)). When measured on the oscilloscope, the output period was found to be , which meant that the frequency was 188.7kHz, which is within the expected range. The ratio of positive to negative pulse width was measured, with the positive width found to be and the negative . Ideally, these would have the same value, but the unequal ratio was not found to be overly problematic. The rise time and fall time were also measured, and found to be **get values**

As before, the voltage and current into the circuit and the AC ripple were again measured, to see if they had changed given the expansion of the circuit. **They were found not to have deviated significantly.**

|  |  |  |
| --- | --- | --- |
| **Value** | **Expected** | **Measured** |
| Circuit voltage | 12V | 12.8V |
| Circuit current | ----- | 29mA |
| Positive pulse width | ----- | 2.9μs |
| Negative pulse width |  | 2.4μs |
| Output frequency | 159 -> 365 kHz | 188.7kHz |
| Output Period | 1/159k -> 1/365k seconds | 5.3μs |
| Rise time | ---- |  |
| Fall time | ---- |  |

Table 4: Test Results for relaxation oscillator

## Counter

Testing at this stage of the circuit involved determining the output frequencies of each of the 8 output pins of the counter and comparing these frequencies to expected values.

Frequencies were calculated using the equation:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Output** | **Calculated Frequency (Hz)** | **Measured Frequency (Hz)** | **Difference**  **(Hz)** | **Difference**  **(%)** |
| Bit 1 (O/p A0) | 188,700 / 2 = 94,350 | 95,700 | + 1350 | 1.4 |
| Bit 2 (O/p A1) | 188,700 / 4 = 47,175 | 47,000 | -175 | 0.3 |
| Bit 3 (O/p A2) | 188,700 / 8 = 23,587 | 23,900 | +313 | 1.3 |
| Bit 4 (O/p A3) | 188,700 / 16 = 11,794 | 11,900 | +196 | 0.9 |
| Bit 5 (O/p A4) | 188,700 / 32 = 5,897 | 5,980 | +83 | 1.4 |
| Bit 6 (O/p A5) | 188,700 / 64 = 2,984 | 3,000 | +16 | 0.5 |
| Bit 7 (O/p A6) | 188,700 / 128 = 1,474 | 1,490 | +16 | 1.1 |
| Bit 8 (O/p A7) | 188,700 / 256 = 737 | 747 | +10 | 1.3 |

Table 5: Test Results for 8-bit Counter

AC Noise was again measured at this point and found to be approx. 25mV, and power consumption was calculated from the input voltage and current and found to be 0.36 Watts.

## Ramp Generator

The ramp generator was tested by measuring the resistance values throughout and across the circuit and comparing them to expected calculated values. If the resistance values were found to be correct, then it is assumed that the voltage values contributing to the ramp will be correct.

|  |  |  |  |
| --- | --- | --- | --- |
| **Test Point 1** | **Calculated Value** | **Measured Value** | **Difference (%)** |
| GND to A0 | 20kΩ | 19.68kΩ | 1.61 |
| GND to A1 | 25kΩ | 24.50kΩ | 2.02 |
| GND to A2 | 30kΩ | 29.42kΩ | 1.95 |
| GND to A3 | 35kΩ | 34.28kΩ | 2.08 |
| GND to A4 | 40kΩ | 39.20kΩ | 2.02 |
| GND to A5 | 45kΩ | 44.10kΩ | 2.02 |
| GND to A6 | 50kΩ | 49.01kΩ | 1.99 |
| GND to A7 | 55kΩ | 53.98kΩ | 1.87 |

Table 6: Measured and calculated resistances across R2R ladder

|  |  |  |  |
| --- | --- | --- | --- |
| **Test Point 2** | **Calculated Value** | **Measured Value** | **Difference (%)** |
| A0 to A1 | 25kΩ | 24.49kΩ | 2.06 |
| A1 to A2 | 25kΩ | 24.42kΩ | 2.34 |
| A2 to A3 | 25kΩ | 24.41kΩ | 2.38 |
| A3 to A4 | 25kΩ | 24.41kΩ | 2.38 |
| A4 to A5 | 25kΩ | 24.43kΩ | 2.31 |
| A5 to A6 | 25kΩ | 24.42kΩ | 2.23 |
| A6 to A7 | 25kΩ | 24.50kΩ | 2.02 |
| A7 to A0 | 55kΩ | 53.80kΩ | 2.21 |

Table 7: Measured and calculated resistances within R2R ladder

In addition, the output ramp voltage was checked on the oscilloscope to ensure that it was outputting the correct shape and magnitude sawtooth wave. As seen below, the output voltage was found to be a 5V sawtooth wave as expected, and the step size was found to be approximately 20mV:

A close up of a map

Description automatically generated

Figure 2: Ramp output of R2R ladder

A close up of a map

Description automatically generated

Figure 3: Individual step size in ramp output

AC Noise was again measured at this point and found to have increased significantly from 25mV to approx. 60mV with the addition of the R2R ladder to the circuit.

## Comparator

## Embedded Interface

## Coding

# Conclusion

**Show the reader what you’ve learned, without adding any new ideas or circuit components.**

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# Appendix

## Calculations for Relaxation Oscillator frequency

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Description automatically generated

# Notes

Recovery diode (D1) in voltage regulator

Labview

Ripple/Noise

Circuits in Multisim to printout

Appendix of board progress?

Table of power drawn and AC noise in appendix?